Docket No. 204612US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yuuichi HIRANO, et al.
SERIAL NO: NEW APPLICATION GAU:
FILED: Herewith EXAMINER:
FOR: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

INFORMATION DISCLOSURE/RELATED CASE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:
Applicant(s) wish to disclose the following information.

REFERENCES

☐ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.

☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

☐ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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STATEMENT OF RELEVANCY

Reference AO (5-251647) on Form PTO-1449:

Fig. 7 shows a semiconductor device having a plurality of p MOSFETs and a plurality of n MOSFETs formed on an SOI substrate. Adjacent ones of the p MOSFETs and adjacent ones of the n MOSFETs are isolated by partial isolation type element isolation insulating films, respectively. Further, one of p MOSFETs and one of n MOSFETs adjacent to each other are isolated by a complete isolation type element isolation insulating film.